CLAIMS

1. A nonvolatile switch comprising:

an input terminal;

an output terminal;

a selection terminal;

a first and a second biasing terminal;

a memory element of flash type, having a first conduction region connected to said first biasing terminal and a second conduction region connected to said second biasing terminal;

a pass transistor, having a first conduction region connected to said input terminal and a second conduction region connected to said output terminal; and

a pair of common-gate regions, having a common floating gate region and a common control gate region, which are capacitively coupled together, said memory element and said pass transistor sharing said common-gate regions, and said common control-gate region being connected to said selection terminal.

2. The switch according to claim 1, further comprising a second pass transistor, having a first conduction region connected to an own input terminal and a second conduction region connected an own output terminal, said second pass transistor, said memory element and said pass transistor sharing said common-gate regions.

3. The switch according to claim 1 wherein said common gate regions extend parallel to one another on top of said body of semiconductor material.

4. The switch according to claim 3 wherein said body accommodates a first and a second active area separated by an insulating region, said common-gate regions extending in a direction transverse to, and on top of, said first and second active

areas, said first active area forming said first and second conduction regions of said memory element, and said second active area forming said first and second conduction regions of said pass transistor.

5. The switch according to claim 4 wherein said body accommodates a third active area forming a third and a fourth conduction region of said pass transistor, said common-gate regions extending in a direction transverse to, and on top of, said third active area, said first and third conduction regions of said pass transistor being electrically connected by a first line of conductive material, extending on top of said body, said second and fourth conduction regions of said pass transistor being electrically connected by a second line of conductive material, extending on top of said body, said first and second line of conductive materials being arranged on opposite sides of said common-gate regions and being connected to respective biasing lines, which extend parallel to each other on top of, and transverse to, said common-gate regions.

6. The switch according to claim 4 wherein said body accommodates a fourth active area forming a first and a second conduction region of a second pass transistor, said common-gate regions extending in a direction transverse to, and on top of, said fourth active area.

7. The switch according to claim 6 wherein said body accommodates a fifth active area forming a third and a fourth conduction region of said pass transistor, said common-gate regions extending in a direction transverse to, and on top of, said fifth active area, said first and third conduction regions of said second pass transistor being electrically connected by a third line of conductive material, extending on top of said body, said second and fourth conduction regions of said second pass transistor being electrically connected by a fourth line of conductive material, extending on top of said body, said third and fourth lines of conductive material being arranged on opposite

sides of said common-gate regions and being connected to respective biasing lines, extending parallel to each other on top of, and transverse to, said common-gate regions.

8. A nonvolatile programmable-logic device comprising:

an input terminal;

an output terminal;

a selection terminal;

a first and a second biasing terminal;

a memory element of flash type, having a first conduction region connected to said first biasing terminal and a second conduction region connected to said second biasing terminal;

a pass transistor, having a first conduction region connected to said input terminal and a second conduction region connected to said output terminal;

a pair of common-gate regions, having a common floating gate region and a common control gate region, which are capacitively coupled together;

a data input connected to said input terminal;

a data output connected to said output terminal; and

a first, a second, and a third biasing generator connected, respectively, to said first, second and selection terminal;

said memory element and said pass transistor sharing said common-gate regions, and said common control-gate region being connected to said selection terminal.

9. A method for controlling a nonvolatile switch comprising a memory element of flash type and a pass transistor, which have a common floating gate region and a common control gate region said method comprising the steps of:

program biasing said common control gate region of said memory element and said pass transistor so as to inject or extract charges into/from said common floating-gate region; and

selection biasing said common control gate region of said memory element and said pass transistor and supplying a datum to an input terminal of said pass transistor during an operating step of said switch.

10. The control method according to claim 9 wherein said step of program biasing comprises:

applying a first and a second potential, respectively, to a first and a second conduction region of said memory element, and applying a third potential to said common control gate region of said memory element and of said pass transistor in a writing step;

leaving said first conduction region of said memory element floating, applying a fourth potential to said second conduction region of said memory element, and applying a fifth potential to said common control gate region of said memory element and of said pass transistor in an erasing step; and

leaving said first conduction region of said memory element floating, applying a reference potential to said second conduction region of said memory element, applying a sixth potential to said common control gate region of said memory element and said pass transistor, and detecting possible data on an output terminal of said pass transistor.